Reset noise reduction architectures for the detection of charged particles

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Abstract

This paper presents a parametric test sensors designed in a 0.18 μm advanced CMOS Image Sensor process. The sensor includes a number of subarrays with different pixel architectures optimised for low noise. These architectures exploit design techniques to achieve noise lower than the reset noise floor and they are suitable for a straightforward implementation in a radiation resistant sensor, as required in many scientific applications. The sensor was fabricated on a P-type epitaxial substrate, in both 5 and 12 μm thickness. Noise as low as 6 e^- rms was demonstrated.

Introduction

Noise is a parameter of paramount importance in image sensors[1]. In addition to this, a number of scientific applications, e.g. nuclear and particle physics [2] or beta-autoradiography [3] in medical imaging, requires imaging of charged particles. These particles damage the sensors thus limiting its lifetime[4].

When traversing a material, charged particles loose energy at a rate ΔE that depends on their energy and mass, and generate a number of electron-hole pairs given by N= ΔE/W, where W=3.6 eV/pair for silicon. If the energy of a particle is sufficiently high, a minimum amount of ionization is produced at a uniform rate, which is equal to about 80 pairs per traversed micron in silicon. Given the thickness of epitaxial layers in CMOS sensors, this corresponds to a small signal which subsequently demands low-noise for efficient detection, together with radiation hardness to insure a viable lifetime for the sensor.

In modern digital cameras, 4T pixels or similar structures are a favourite solution because they allow Correlated Double Sampling (CDS) and can achieve very low noise [5]. However, little data exist in the literature regarding the radiation resistance of these

[1] See for example papers in sessions 12 and 19 at previous 2007 edition of this workshop http://www.imagesensors.org/Past%20Workshops/2007%20Workshop/Hyperlinked%20Contents.htm

[2] P. Allport et al., *R&D on Monolithic Active Pixel Sensors (MAPS): towards large-area CMOS sensors for particle physics*, *Nucl. Instruments and Methods in Physics Research A*, vol. 573, 16-18, 2007

[3] J. Cabello et al, *Digital autoradiography using room temperature CCD and CMOS imaging technology*, 2007 Physics in Medicine and Biology, vol. 52, 4993-5011

[4] G.C. Messenger, M.S. Ash, *The Effects of Radiation on Electronic Systems*, New York, 1992.

[5] A. Krymski, N. Khaliullin, H. Rhodes, *A 2 electron noise, 1.3 Megapixel CMOS Sensor*, Proc. 2003 IEEE Workshop on CCDs and Advanced Image Sensors, May 15-17, 2003 Bavaria, Germany

pixels[6]. We subsequently decided to develop low noise pixels by using design techniques. Although the sensor presented here is not designed for radiation hardness, known design techniques [7] [8] exist that would allow a straightforward implementation of a rad-hard version.

We designed a parametric test sensor, eLeNA (Low Noise APS, Figure 1), which consists of an array of fourteen different pixel designs, arranged over 512 rows and 448 columns. The sensor was designed in a 0.18 μm, advanced CIS process which also includes a novel module, a deep P-well, for which more details are given in another paper[9]. The pitch of the array is 15 μm, which is relatively large compared to consumer applications, but well matched to the requirements of a number of scientific applications[10].

The pixel subarrays include: 3T pixels as reference designs; pixels with clamping capacitors for CDS; pixels with active reset[11]; pixels with sampling capacitors. All pixels use standard devices. Details on all the pixels were presented in a paper submitted to the recent issue on imaging devices for the IEEE Trans. on Electron Devices. Here we focus on two of them.

The first architecture is the pixel with clamping capacitors. This was previously described[12] and the schematic of the pixel as well as its timing diagram are shown in Figure 2 and Figure 3 respectively. This version achieves good noise performance but suffers from a high power consumption. In order to improve on this we modified the design (Figure 4). The added transistors controlled by the 'write' signal allow the 1st source follower to be switched off when not in use.

Pixels with sampling capacitors are particularly interesting for particle detection because they allow CDS as well as snapshot, an important characteristic for some applications where the integration period must be the same for all the pixels, i.e. no rolling shuttle or scan readout allowed. The schematic and timing of this pixel are shown in Figure 5 and Figure 6 respectively. Two different layouts, named D1 and D2, were implemented with the same topology. Their design characteristics are shown in Table 1. Two variants were designed, D1 and D2, which differs mainly for the size of the capacitors. Experimental noise and gain distributions are shown in Figures 7 and 8, showing a most probable value for the noise of

[6] P. Rao et al., *Degradation of CMOS image sensors in deep-submicron technology due to γ-irradiation*, Solid-State Electronics 52 (2008) 1407–1413

[7] W. Snoeys et al., *Layout techniques to enhance the radiation tolerance of standard CMOS technologies demonstrated on a pixel detector readout chip*, Nucl. Instrum. and Methods, vol. A439, pp. 349–360, Jan. 2000.

[8] W. J. Snoeys, T. A. Palacios Gutierrez, G. Anelli, *A new NMOS layout structure for radiation tolerance*. IEEE Trans Nucl Sci 2002;49(4):1829–33

[9] J. Ballin et al., *An advanced CMOS Active Pixel Sensor in a novel quadruple well process (INMAPS) for a 100% Fill Factor and Full CMOS Pixels*, these Proceedings

[10] R. Turchetta et al., *CMOS Monolithic Active Pixel Sensors (MAPS): Developments and future outlook*, Nucl. Instrum. and Methods, vol. A582 (2007) pp. 866–870

[11] B. Pain et al., *Reset noise suppression in two-dimensional CMOS photodiode pixels through column-based feedback-reset*, in Proc. 2002 IEDM, 2002, pp. 809–811

[12] S. Kleinfelder et al., *Novel Integrated CMOS Sensor Circuits*, IEEE Trans. On Nuclear Science, vol. 51 (5) 2328-2339

about 6 e- rms and good agreement with the design parameters (see Table 2). It has to be noticed that the capacitor as well as other active devices do not alter the fill factor for the detection of charged particle, provided no other P-N junction than the one of the collecting diode is integrated in the sensor[13].

Conclusion

This paper describes a parametric test sensor aiming at achieving low noise with design techniques. The advantage of this methodology is that known design techniques exist for achieving good radiation resistance.

The sensor consists of 512 x 448 pixels at 15 mm pitch and was designed in a 0.18 µm CIS technology. Fourteen different variants were designed. This paper focuses on two of them which share the same topology with two source followers separated by a sampling capacitor. Noise as low as 6 e- rms was achieved.

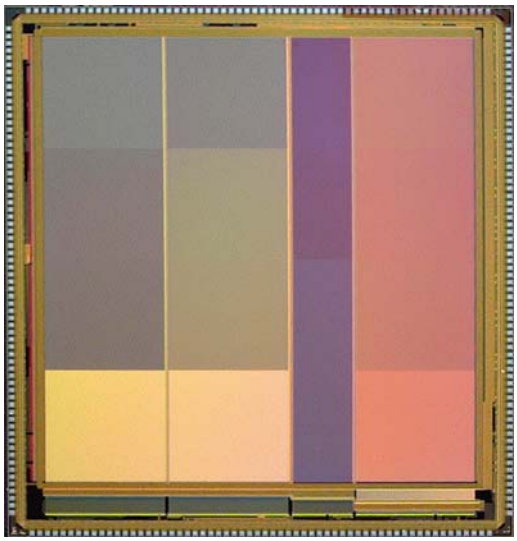

Figure 1. Microphotograph of eLeNA

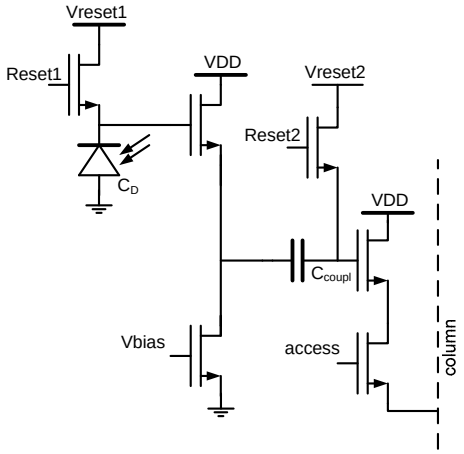

Figure 2. Schematic of the InPixelCDS pixel.

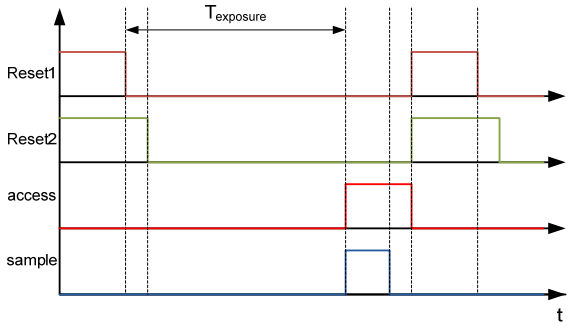

Figure 3. Signal arrangement for the InPixelCDS pixel.

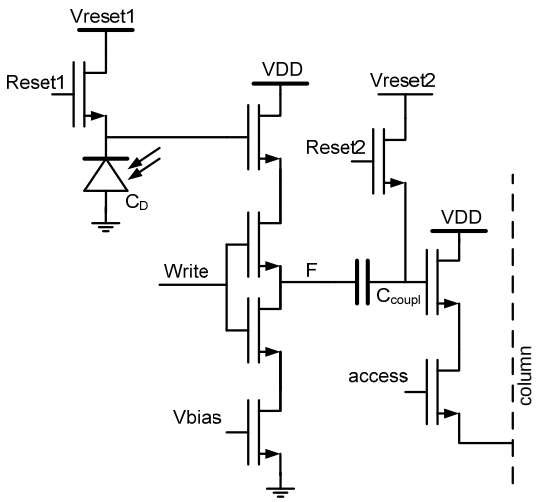

Figure 4. Schematic of the improved InPixelCDS pixel.

[13] J. Ballin et al., *Monolithic Active Pixel Sensors (MAPS) in a Quadruple Well Technology for Nearly 100% Fill Factor and Full CMOS Pixels*, Sensors 2008, 8(9), 5336-5351; Special Issue on Integrated High-performance Imagers

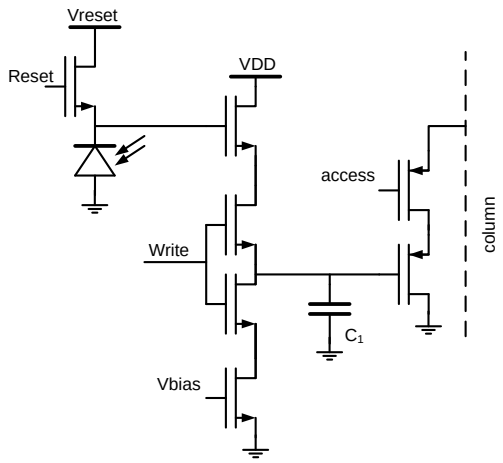

Figure 5. Schematic of the improved CDS2Sample pixel.

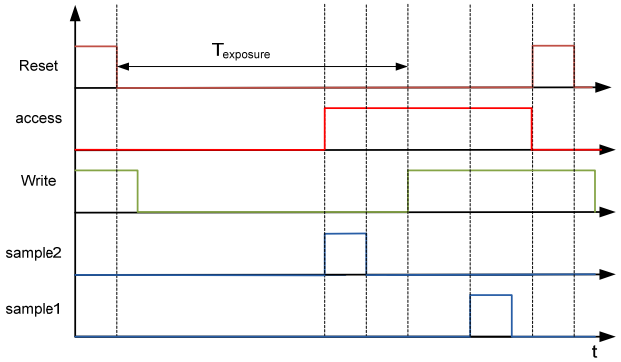

Figure 6. Timing or the CDS2Sample pixel.

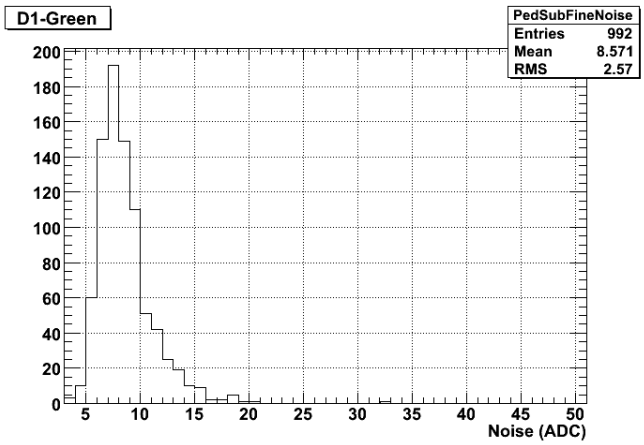

Figure 7. Noise for CDS two sample (D1) 12µ epi

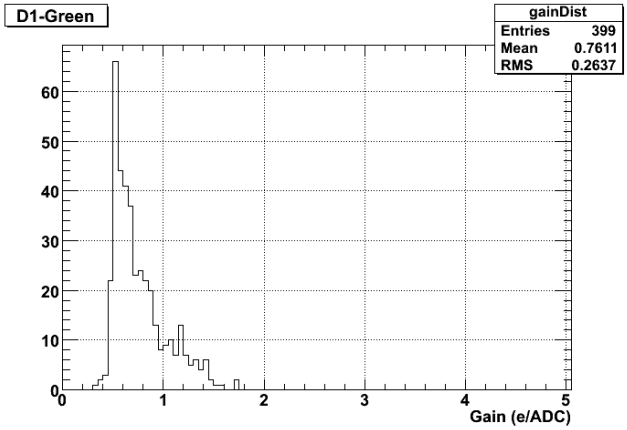

Figure 8. Gain Distribution for CDS two sample (D1) 12µ epi

Quantity	D1	D2
C_1 (fF)	252	69
Total Chip Gain (simulated)	0.575	0.575
Input referred reset noise (mV rms)	1.3	1.3
Conversion gain (µV/e-)	39	39
Total Noise Without CDS (e-rms)	207	200
Simulated output Noise (mV rms)	0.225	0.35
Simulated output Noise (e-rms)	5.7	10
Hand Calculated Noise (e-rms)	3.33	5.5

Table 1. Design parameters for the pixel with sampling capacitor.

Quantity	Unit	D1	D2
Gain	µV/e	33.0	28.0
Noise	e rms	6.4	9.5
Noise Reduction Factor		10.9	8.8
FW linear		12,500	12,167
Dynamic range linear		1959	1285
Dynamic range linear	dB	65.8	62.2
Dynamic range linear	Bit	10.9	10.3
FPN @ 0 signal	e	21.6	27.26
Dark current	e / sec	500	NA

Table 2. Measured parameters for the pixel with sampling capacitor.